WHAT IS CLAIMED IS:

1. A magnetoresistive random access memory device comprising:

a magnetic memory cell which includes a first magnetoresistive element, a second magnetoresistive element and at least one transfer gate connected in series to the first and second magnetoresistive element,

each of the first and second magnetoresistive element having a tunnel magnetoresistive effect and the first and second magnetoresistive element being inserted between both ends of the magnetic memory cell;

a pair of first bit lines connected to the magnetic memory cell;

a first word line disposed so as to face closely to the magnetic memory cell; and

a second bit line connected to the magnetic memory cell.

2. The magnetoresistive random access memory device according to claim 1, wherein the first and second magnetoresistive elements hold two data items of opposite logic levels, respectively.

3. The magnetoresistive random access memory device according to claim 1, wherein the pair of first bit lines applies a specific potential difference to both the ends of the magnetic memory cell when reading data, and

the magnetic memory cell reads the potential determined by a ratio of the combined resistance of the first magnetoresistive element and the second magnetoresistive element to the resistance of the first magnetoresistive element or the second magnetoresistive element onto the second bit line.

4. The magnetoresistive random access memory device according to claim 1, wherein said at least one transfer gate includes a first and a second transfer gate which each have a gate electrode and are connected in series between the first and second magnetoresistive elements,

the magnetoresistive random access memory further comprising a second word line which is connected to both the gate electrodes of the first and second transfer gates.

5. The magnetoresistive random access memory device according to claim 4, wherein the second word line is activated when reading data.

6. The magnetoresistive random access memory device according to claim 1, wherein said at least one transfer gate includes:

a first transfer gate which has a gate electrode and is connected between one of both the ends of the magnetic memory cell and the first magnetoresistive element; and

a second transfer gate which has a gate

electrode and is connected between the other of both the ends of the magnetic memory cell and the second magnetoresistive element,

the magnetoresistive random access memory further comprising a second word line connected to both the gate electrodes of the first and second transfer gates.

7. The magnetoresistive random access memory device according to claim 6, wherein the second word line is activated when reading data.

8. The magnetoresistive random access memory device according to claim 1, wherein said at least one transfer gate includes a first transfer gate which has a gate electrode and is connected between the first magnetoresistive element and the second magnetoresistive element, and a second transfer gate which has one end, the other end, and a gate electrode, with one end connected to a junction point of the first magnetoresistive element and the first transfer gate and the other end connected to the second bit line,

the magnetoresistive random access memory further comprising:

a third transfer gate which has one end, the other end, and a gate electrode, with one end connected to a junction point of the second magnetoresistive element and the first transfer gate and the other end connected to the second bit line; and

a second word line connected to the gate

electrodes of the first, second and third transfer gates.

9. The magnetoresistive random access memory device according to claim 8, wherein the second word line is activated when reading data.

10. The magnetoresistive random access memory device according to claim 1, wherein said at least one transfer gate includes a first transfer gate which has a gate electrode and is connected between the first magnetoresistive element and the second magnetoresistive element,

the magnetoresistive random access memory further comprising:

a second transfer gate which has a gate electrode and is connected between a junction point of either the first magnetoresistive element or the second magnetoresistive element and the first transfer gate and the second bit line; and

a second word line connected to the gate electrodes of the first and second transfer gates.

11. The magnetoresistive random access memory device according to claim 10, wherein the second word line is activated when reading data.

12. The magnetoresistive random access memory device according to claim 1, further comprising a sense amplifier which is connected to the second bit line and compares a potential of the second bit line with

a reference potential to sense data.

13. The magnetoresistive random access memory device according to claim 12, wherein the reference potential is an intermediate potential between a first potential applied to one of both the ends of the magnetic memory cell and a second potential applied to the other of both the ends of the magnetic memory cell when reading data.

14. The magnetoresistive random access memory device according to claim 12, further comprising a reference potential generator circuit which is connected to the sense amplifier and generates the reference potential.

15. The magnetoresistive random access memory device according to claim 14, wherein the reference potential generator circuit includes a dummy magnetic memory cell which is composed of magnetoresistive elements similar to those in the magnetic memory cell and generates the reference potential, and

a third bit line onto which the reference potential generated by the dummy magnetic memory cell is read.

16. The magnetoresistive random access memory device according to claim 15, wherein the dummy magnetic memory cell includes:

a first dummy cell composed of two dummy magnetoresistive elements holding data items of

opposite logic levels, respectively;

a second dummy cell composed of two dummy magnetoresistive elements holding data items of opposite logic levels, respectively, and of reverse logic levels to those logic levels in the first dummy cell; and

a potential combining circuit to combine the potentials read from the first and second dummy cells and generate the reference potential.

17. The magnetoresistive random access memory device according to claim 15, wherein the dummy magnetic memory cell includes:

a first dummy cell composed of two dummy magnetoresistive elements holding data items of similar logic levels;

a second dummy cell composed of two dummy magnetoresistive elements holding data items of similar logic levels reverse logic levels to those logic levels in the first dummy cell; and

a potential combining circuit to combine the potentials read from the first and second dummy cells and generate the reference potential.

18. The magnetoresistive random access memory device according to claim 1, further comprising:

a switching circuit which applies a first potential difference between both the ends of the magnetic memory cell in a first period when reading

data, and which applies a second potential difference which has the same magnitude as the first potential difference and opposite in polarity to the first potential difference between both the ends of the magnetic memory cell in a second period when reading data; and

a read circuit which uses the potential read onto the second bit line from the magnetic memory cell in the first period as a reference potential and compares the potential read onto the second bit line from the magnetic memory cell in the second period with the reference potential to sense data.

19. The magnetoresistive random access memory device according to claim 1, further comprising:

a first switching circuit which applies a first potential difference between both the ends of the magnetic memory cell in a first period when reading data, and which applies a second potential difference which has the same magnitude as the first potential difference and opposite in polarity to the first potential difference between both the ends of the magnetic memory cell in a second period when reading data;

a second switching circuit which outputs a potential read onto the second bit line from the magnetic memory cell in such a manner that the output is switched between the first period and the second

period; and

a sense amplifier which holds the potential output from the second switching circuit in the first period as a reference potential and compares the potential output from the second switching circuit in the second period with the reference potential to sense data.

20. The magnetoresistive random access memory device according to claim 1, further comprising:

a switching circuit which applies a first potential difference between both the ends of the magnetic memory cell in a first period when reading data, and which applies a second potential difference which has the same magnitude as the first potential difference and opposite in polarity to the first potential difference between both the ends of the magnetic memory cell in a second period when reading data;

a first switch element which has one end and the other end, with one end connected to the second bit line, and which is switched on temporarily in the first period and is switched on temporarily in the second period;

a sense amplifier which is connected to the other end of the first switch element and senses a change in a potential input via the first switch element to sense data; and

a second switch element which is connected between

an input and an output nodes of the sense amplifier and which is switched on in the first period and is switched on temporarily in the second period.

21. A magnetoresistive random access memory device comprising:

a memory cell array including a plurality of magnetic memory cells arranged in rows and columns, each magnetic memory cell having a first magnetoresistive element, a second magnetoresistive element and at least one transfer gate connected in series to the first and second magnetoresistive elements, each of the first and second magnetoresistive elements having a tunnel magnetoresistive effect and the first and second magnetoresistive elements being inserted between both ends of the magnetic memory cell;

a plurality of first word lines connected to a plurality of magnetic memory cells provided in each row in the memory cell array;

a plurality of first bit lines connected to a plurality of magnetic memory cells provided in each column in the memory cell array; and

a plurality of sense amplifiers which are provided for the individual columns in the memory cell array and are connected to the corresponding ones in a plurality of first bit lines.

22. The magnetoresistive random access memory device according to claim 21, wherein the first and

second magnetoresistive elements hold two data items of opposite logic levels, respectively.

23. The magnetoresistive random access memory device according to claim 22, wherein a specific potential difference is applied between both ends of each of said plurality of magnetic memory cells when reading data, and

each of said plurality of magnetic memory cells reads the potential determined by a ratio of a combined resistance of the first magnetoresistive element and the second magnetoresistive element to the resistance of the first magnetoresistive element or the second magnetoresistive element onto the first bit line.

24. The magnetoresistive random access memory device according to claim 22, wherein said at least one transfer gate includes a first and a second transfer gates which each have a gate electrode and are connected in series between the first and second magnetoresistive elements,

the magnetoresistive random access memory further comprising a second word line which is connected to the gate electrodes of the first and second transfer gates and is activated when reading data.

25. The magnetoresistive random access memory device according to claim 22, wherein said at least one transfer gate includes:

a first transfer gate which has a gate electrode

and is connected between one of both the ends of the magnetic memory cell and the first magnetoresistive element; and

a second transfer gate which has a gate electrode and is connected between the other of both the ends of the magnetic memory cell and the second magnetoresistive element,

the magnetoresistive random access memory further comprising a second word line which is connected to the gate electrodes of the first and second transfer gates and is activated when reading data.

26. The magnetoresistive random access memory device according to claim 22, wherein said at least one transfer gate includes a first transfer gate which has a gate electrode and is connected between the first magnetoresistive element and the second magnetoresistive element,

the magnetoresistive random access memory further comprising:

a second transfer gate which has one end, the other end, and a gate electrode, with one end connected to a junction point of the first magnetoresistive element and the first transfer gate and the other end connected to the bit line;

a third transfer gate which has one end, the other end, and a gate electrode, with one end connected to a junction point of the second magnetoresistive element

and the first transfer gate and the other end connected to the bit line; and

a second word line which is connected to the gate electrodes of the first, second and third transfer gates and is activated when reading data.

27. The magnetoresistive random access memory device according to claim 22, wherein said at least one transfer gate includes a first transfer gate which has a gate electrode and is connected between the first and second magnetoresistive elements,

the magnetoresistive random access memory further comprising:

a second transfer gate which has a gate electrode and is connected between a junction point of either the first magnetoresistive element or the second magnetoresistive element and the first transfer gate, and the second bit line; and

a second word line which is connected to the gate electrodes of the first and second transfer gates and is activated when reading data.

28. The magnetoresistive random access memory device according to claim 22, wherein said plurality of sense amplifiers are connected to said plurality of first bit lines and each compares the potential of the corresponding one of said plurality of first bit lines with the reference potential to sense data.

29. The magnetoresistive random access memory

device according to claim 28, wherein the reference potential is an intermediate potential between a first potential applied to one of both the ends of magnetic memory cell and a second potential applied to the other of both the ends of the magnetic memory cell when reading data.

30. The magnetoresistive random access memory device according to claim 28, further comprising a plurality of reference potential generator circuits to generate the reference potential.

31. The magnetoresistive random access memory device according to claim 30, wherein each of said plurality of reference potential generator circuits includes:

a dummy magnetic memory cell which is composed of magnetoresistive elements similar to those in each of said plurality of magnetic memory cells and generates the reference potential; and

a second bit line onto which the reference potential generated by the dummy magnetic memory cell is read.

32. The magnetoresistive random access memory device according to claim 31, wherein the dummy magnetic memory cell includes:

a first dummy cell composed of two dummy magnetoresistive elements holding data items of opposite logic levels, respectively;

a second dummy cell composed of two dummy magnetoresistive elements holding data items of opposite logic levels, respectively, and of reverse logic levels to those logic levels in the first dummy cell; and

a potential combining circuit to combine the potentials read from the first and second dummy cells to generate the reference potential.

33. The magnetoresistive random access memory device according to claim 31, wherein the dummy magnetic memory cell includes;

a first dummy cell composed of two dummy magnetoresistive elements holding data items opposite logic levels, respectively;

a second dummy cell composed of two dummy magnetoresistive elements holding data items of similar logic levels reverse logic levels to those logic levels in the first dummy cell; and

a potential combining circuit to combine the potentials read from the first and second dummy cells to generate the reference potential.

34. The magnetoresistive random access memory device according to claim 28, further comprising a reference potential generator circuit which is connected to said plurality of sense amplifiers and generates the reference potential.

35. The magnetoresistive random access memory

device according to claim 34, wherein the reference potential generator circuit is composed of a plurality of dummy magnetic memory cells for a column provided in the memory cell array.

36. The magnetoresistive random access memory device according to claim 23, further comprising a plurality of drivers which are provided for the individual columns in the memory cell array and supply the specific potential difference between both the ends of each of a plurality of magnetic memory cells in each column in the memory cell array before reading data.

37. The magnetoresistive random access memory device according to claim 36, wherein each of said plurality of drivers includes:

a first transistor to apply a first potential to one of both the ends of each of a plurality of magnetic memory cells in each column in the memory cell array; and

a second transistor to apply a second potential to the other of both the ends of each of said plurality of magnetic memory cells in each column in the memory cell array.

38. The magnetoresistive random access memory device according to claim 36, wherein each of said plurality of drivers is provided at one end of the memory cell array in the column direction.

39. The magnetoresistive random access memory

device according to claim 36, wherein each of said plurality of drivers precharges both the ends of a plurality of magnetic memory cells in each column in the memory cell to specific potentials before reading data.

40. The magnetoresistive random access memory device according to claim 22, wherein each of said plurality of first bit lines is precharged to a specific potential, before reading data.